HIGH POWER DISTRIBUTED AMPLIFIER USING MBE SYNTHESIZED MATERIAL*

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ABSTRACT

The main limitations of the output power of a distributed amplifier are the gate line loss and the gate-to-drain breakdown voltage. A novel circuit concept to reduce the gate loss using series capacitors on the gate feeding lines has been implemented. The device breakdown voltage has been improved by using an MBE grown material with two layers (low doped gate buffer layer and usual active layer). A monolithic GaAs distributed amplifier using 6 x 300 μm FETs has achieved an output power of 800 mW with 4dB gain. The power added efficiency was about 15 %.

INTRODUCTION

Recently, the GaAs FET device technology and monolithic circuit implementation technique have been combined successfully for the development of ultra-broadband distributed amplifier.[1,2,3,4] But the power performance of the amplifier was limited by the gate line loss and gate-to-drain breakdown voltage. Those limitations have been improved using a novel circuit concept and device structure. To reduce the gate line loss per unit gate width, series capacitors have been implemented on the gate feeding lines of a distributed amplifier. The device breakdown voltage has been increased using an MBE grown material with two active layers: n⁻ gate buffer layer followed by an n active layer. As shown below, the resulting distributed amplifier improved the power performance significantly.

CIRCUIT DESIGN

For a GaAs FET distributed amplifier, it can be shown that the gate and drain attenuation coefficients, α_g and α_d, are given by [5,6].

$$\alpha_g \simeq (\omega C_g)^2 R_g Z_g/2 \quad (1)$$

$$\alpha_d \simeq Z_d/2R_d \quad (2)$$

In equations (1) and (2), Z_g and Z_d are the characteristic impedances of the gate and drain transmission lines. C_g is the input capacitance of an FET. R_g and R_d are input and output resistances of the FET. Due to the input and output resistances, significant losses are incurred. The attenuation of the gate line is particularly severe, due to the frequency dependent squared term. It is this attenuation that limits the maximum number of devices that can be implemented. To reduce the gate-line attenuation, a series capacitor is inserted between the FET gate and the transmission line as shown in Figure 1. The capacitor reduces the effective value of C_g of the gate line, resulting in a decreased α_g.[2] To provide a constant rf voltage across all the FET gates, the series capacitors are tapered. Figure 2 shows the voltage across the gates. It is clearly shown that a fairly constant gate voltage can be maintained with this scheme, even though the input signal at the gate line attenuates significantly.

Significant losses are also incurred at the drain line. For the uniform impedance line at the drain, only half of the current generated flows into the load, and the other half flows into the reverse direction and is dissipated. To increase the gain of a distrtibuted amplifier, the amount of current flowing in the reverse direction should be minimized. This can be achieved using the so-called tapered impedance scheme: the output impedance of the line decreases as a function of 1/n, where n is the section number.[7] The practical implementation of the precise impedance tapering requirement with Z ~ 1/n is difficult to achieve because of the practical restriction of transmission line impedance levels. Instead, a linearly tapered line ranging from 75 to 50 ohm is designed.

At the termination ends of the drain and gate lines, reflectors are added instead of resistive absortion terminations. The terminations are design in such a way that the reflected wave has constructive interference at the high frequency end of operation band, where the amplifier gain and power are lower.

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It is found that the reflectors must generate a phase angle comparable to the propagation phase delay of the incident wave through the amplifier. The reflectors degrade the VSWR of the amplifier. Because of the line attenuations, however, the VSWR degrations are minimal.

DEVICE STRUCTURE OPTIMIZATION

The breakdown of an FET is occured at the drain side edge of a gate and it limits the output power of a distributed amplifier. The voltage has been improved by using an MBE grown material with two active layers: n^- gate buffer layer (1. x $10^{17}/cm^3$) followed by an n active layer (5. x $10^{17}/cm^3$). The layer thicknesses were 0.2 μm and 0.05 μm, respectively. The usual buffer layer was provided under the n layer. To reduce the parasitic resitances, an n^+ contact layer was grown on top of n^- layer. The material structure is depicted in Figure 3. On the material, a 300 μm wide interdigitated FET has been fabricated According to the gate recess depth, the breakdown voltage was varied. As the gate buffer layer thickness increased, the breakdown voltage increased but it reached peak value of 17 volts and started to drop. g_m of the device also varied from 170 mmho/mm to less than 100 mmho/mm. The transconductance at the peak point was 135mmho/mm and was chosen as an optimum gate recess. The breakdown voltage is a significant improvement over the device fabricated on a flat profile material (2 X 10^{17}) with a similar g_m which is about 10~14 volts. The higher breakdown voltage improved the power performance of the distributed amplifier, which would be described in the next section.

EXPERIMENTAL RESULTS

The above-described circuit design technique has been implemented in a 6 X 300 μm monolithic GaAs distributed amplifier design and several slices of this monolithic distributed amplifier have been processed and evaluated. Figure 4 shows a photograph of the amplifier chip. The chip size is 50 X 105 X 4 mils Via holes for source groundings are provided between each of the 300 μm cells. Monolithic resistors shunting the series MIM capacitors are used for gate bias. The distributed amplifier based on flat profile material with doping level of 2.5 x $10^{17}/cm^3$ delivered a linear gain of 5 ± 1 dB across the 2 to 22 GHz frequency range as shown in Figure 5. Under large signal operation and at a higher drain voltage (8 V), this amplifier has produced an output power of 0.5 W with at least 4 dB gain over the 2 to 21 GHz band. The power-added efficiency at 0.5 W output was 14%.

The same distributed amplifier has been fabricated on the two layer material described above. The distributed amplifier delivered an output power of 630 mW with 5 dB gain. Increased rf drive produced an output power of 800 mW with 4 dB gain and 15 % power added efficiency. The optimum drain bias was 9.5 volts. The saturated output power was 1.1 W. The output power was about 2 dB above the distributed amplifier based on a flat doping profile material. This is the highest output power ever achieved for the distributed amplifier without power combining. Improvement in output power is attributed to the higher breakdown voltage.

CONCLUSIONS

A state of the art result for a GaAs distributed power amplifier has been achieved by optimizing the device and circuit concepts. The device based on the low-high two layer material improved the breakdown voltage significantly and so the output power. Due to the changes of the equivalent circuit parameters of the device, the amplifier circuit was not optimum. Because of the lower loss at the gate line, the over all device gate width could be longer. Further improvement in gain is expected with a slight modification of circuits and increasing the over all device size.

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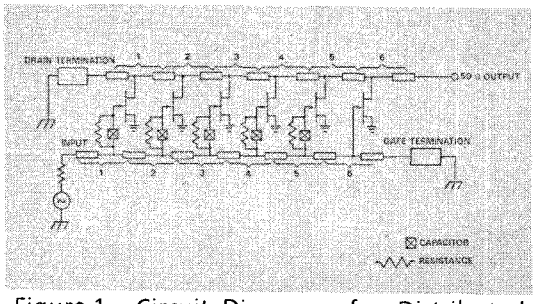

Figure 1. Circuit Diagram of a Distributed Power Amplifier with Tapered Element.

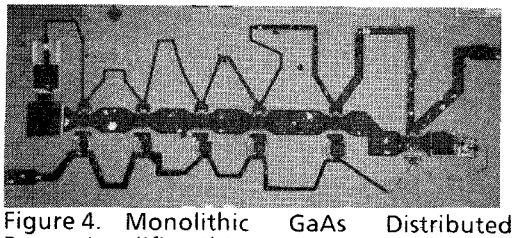

Figure 4. Monolithic GaAs Distributed Power Amplifier Chip.

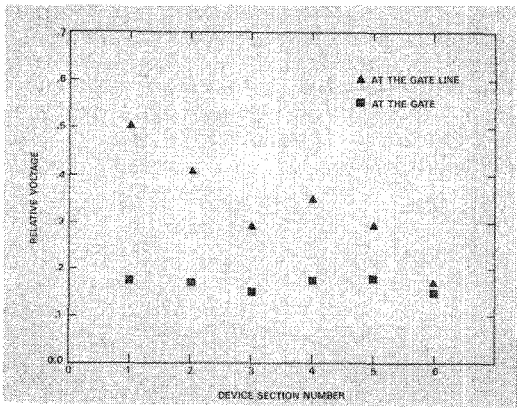

Figure 2. Voltage Distribution at the Gate and at the Gate Line.

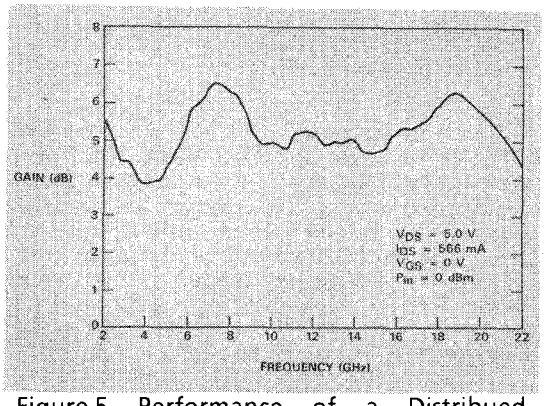

Figure 5. Performance of a Distribued Power Amplifier.

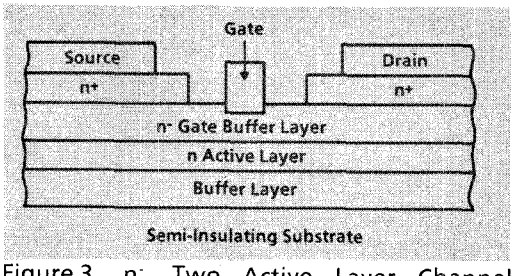

Figure 3. n⁻, Two Active Layer Channel Structure.